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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 10/707,968	Confirmation No.	: 1967
Applicant	: Dominique **MANGELINCK** et al.		
Filed	: January 29, 2004		
TC / A.U.	: 2811		
Examiner	: Not Assigned Yet		
Docket No.	: ASTAP2004-01		
Customer No.	: 031366		
Title	: Gate Electrodes and the Formation Thereof		

CERTIFICATE OF TRANSMISSION
I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, Alexandria, VA 22313-1450 on May 25, 2004.

Signed: Wendy

Wendy LIM

Mail-Stop PCT
Commissioner for Patents
P.O. Box 1450
Alexandria, Va 22313-1450

Petition to convert an application which was filed under 35 U.S.C. § 111(A) to a national application filed under 35 U.S.C. § 371

Sir:

This petition (Petition) is submitted under 37 CFR §1.182 to convert the above-mentioned application (Application) filed under 35 U.S.C. §111(a) to a national stage application filed under 35 U.S.C. §371.

The filing receipt indicates that the Application has been treated as an application filed under 35 U.S.C. §111(a). However, the original intention of the Applicants is to file the Application under 35 U.S.C. §371 as a National Stage Application of International Application No. PCT/SG02/00174 (International Application), filed July 31, 2002, designating the United States of America.

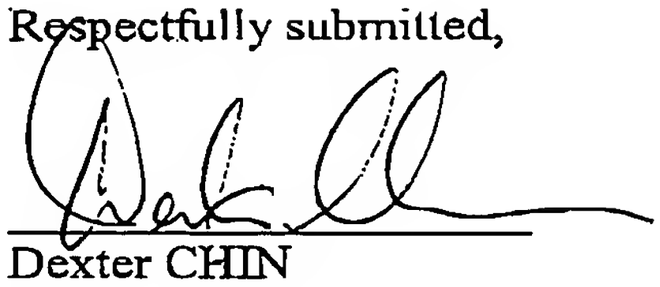
The Application was filed using the Electronic Filing System (EFS), which provided an option on the "continuity data" screen to specify the §371 relationship between the present Application and the prior-filed International Application (*see* Exhibit A). The EFS software (ePAVE) automatically generated an application data sheet that clearly indicates that the Application is a National Stage of the International Application in the "Continuing Data" section (*see* Exhibit B), the International Application being identified by its PCT Application Number and International Filing Date. In addition, a reference to the International Application was provided in the originally filed specification (*see* Exhibit C), clearly indicating that the Application is a National Stage of the International Application.

Accordingly, Applicants respectfully request that the present Application be treated as a filing under 35 U.S.C. §371. Please charge the Petition fee of $130.00 under 37 CFR 1.53(b)(1) to Deposit Account No. 50-2388. The Commissioner is further authorized to charge any additional fees which may be required, or credit any overpayment to this account. Issuance of a corrected formal filing receipt is respectfully solicited.

Appl. No.: 10/707,968
Petition to convert a §111(a) application to a §371 application, dated May 25, 2004
Response to Notice Regarding Benefit/Priority Claim of Mar 23, 2004

Dated: May 25, 2004

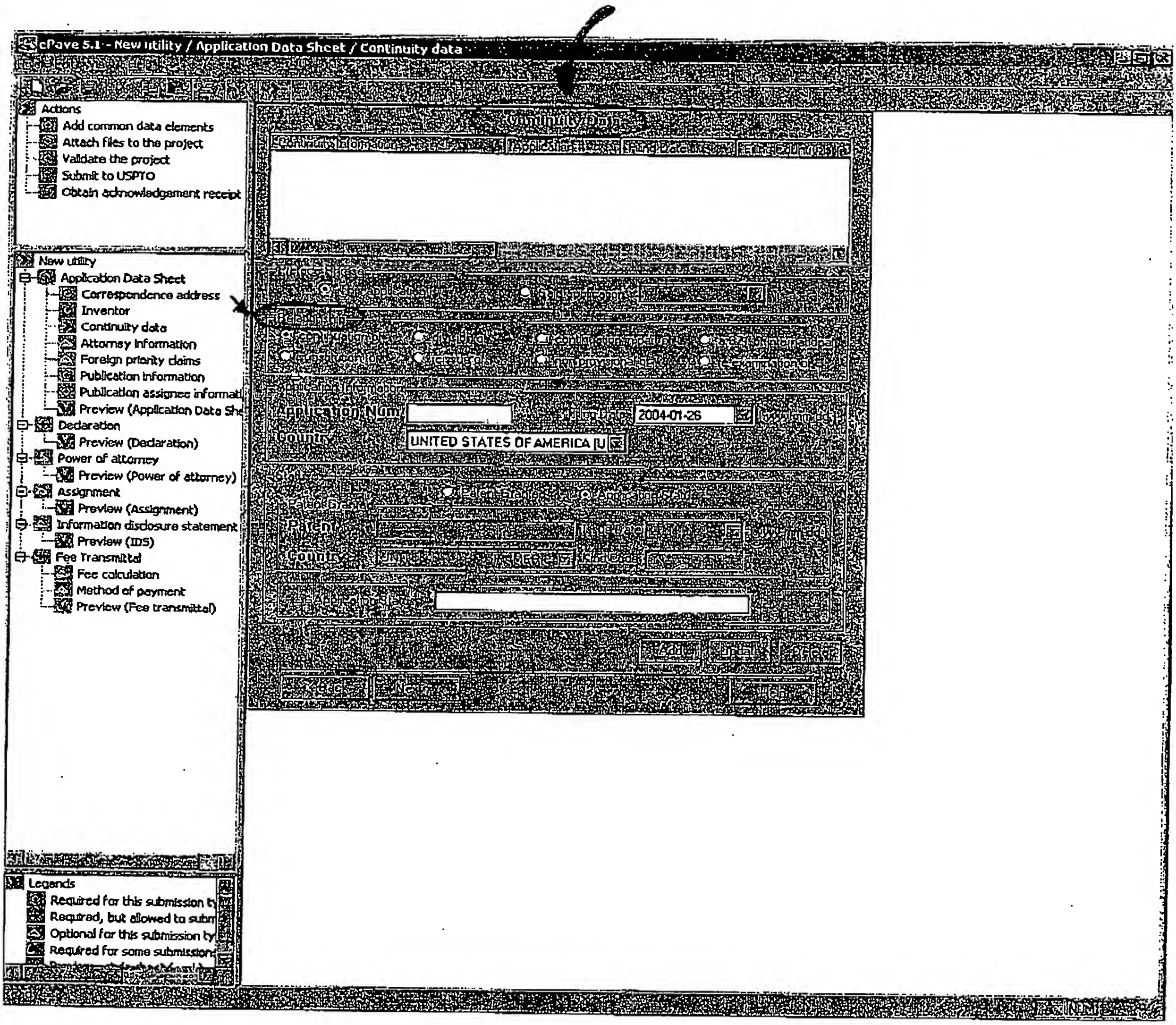
Respectfully submitted,



Dexter CHIN
Attorney for Applicants
Reg. No. 38,842

Horizon IP Pte Ltd
166 Kallang Way,
6th Floor
Singapore 349249
Tel: (65) 9836 9908
Fax: (65) 6746 8263

Exhibit A


cPave 5.1 - New Utility / Application Data Sheet / Continuity data
Actions
Add common data elements
Attach files to the project
Validate the project
Submit to USPTO
Obtain acknowledgement receipt
New utility
Application Data Sheet
Correspondence address
Inventor
Continuity data
Attorney information
Foreign priority claims
Publication information
Publication assignee informati
Preview (Application Data She
Declaration
Preview (Declaration)
Power of attorney
Preview (Power of attorney)
Assignment
Preview (Assignment)
Information disclosure statement
Preview (IDS)
Fee Transmittal
Fee calculation
Method of payment
Preview (Fee transmittal)
Legends
Required for this submission b
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Required for some submission
Continuity Data
Application Num
Filing Date
2004-01-26
Country
UNITED STATES OF AMERICA [U
Parent Data
Parent
Country

US-Request

Exhibit B

APPLICATION DATA SHEET

Electronic Version v14
Stylesheet Version v14.0

Title of Invention	Gate Electrodes and the Formation Thereof

Application Type: regular, utility
Attorney Docket Number: ASTAP2004-01

Correspondence address:

Customer Number: 031366 *031366*

Continuing Data:

This is a National Stage of SG application number PCT/SG02/00174, filed 2002-07-31 , now Published.

Priority Data:

Doc.No: 0104614-3; Country - SG; Date: 2001-07-31 us-priority-claimed

Inventors Information:

Inventor 1:

Applicant Authority Type:	Inventor
Citizenship:	FR
Name prefix:	Mr.
Given Name:	Dominique
Family Name:	Mangelinck
City of Residence:	Marseille
Country of Residence:	FR
Address-1 of Mailing Address:	L2MP, UMR CNRS 6137, Case 151,
Address-2 of Mailing Address:	Faculte de St Jerome, Marseille Cedex 20, France 13397
City of Mailing Address:	Marseille
State of Mailing Address:	
Postal Code of Mailing Address:	13397
Country of Mailing Address:	FR
Phone:	
Fax:	

Exhibit C

SPECIFICATION

[Electronic Version 1.2.8]

GATE ELECTRODES AND THE FORMATION THEREOF

Cross Reference to Related Applications

This application is the National Stage of International Application No. PCT/SG02/00174, filed July 31, 2002, and which was published in English under PCT Article 21(2) as WO 03/012876 A1 on February 13, 2003. The international application claims priority to Singaporean Application No. 200104614-3, filed July 31, 2001.

Background of Invention

[0001] Referring to Figure 1 of the accompanying drawings, a complementary metal oxide semiconductor (CMOS) transistor comprises an n channel MOS (NMOS) and a p channel MOS (PMOS). Historically, a polycrystalline n^+-Si gate is used as a gate electrode both in NMOS and PMOS transistors. For PMOS transistors additional boron implantation into the channel region of the Si substrate is needed to control the threshold voltage because of the low work function of n^+-Si. This can produce short channel effects and large sub-threshold currents and thus the PMOS transistor is less scaleable than the NMOS transistor. In order to solve this problem, a dual gate configuration where polycrystalline n^+-Si and p^+-Si are used as the gate for the NMOS and PMOS transistors, respectively, has been suggested. However, the dual gate CMOS has drawbacks, most notably boron penetration (for PMOS) through the gate oxide and the poly-depletion effect. Instead of using a dual gate, a material with a work function close to the value of the middle of the bandgap of silicon (4.61 eV), can be used for both NMOS and PMOS transistors. A material with such a work function is called a mid-gap material and the process utilising this material for a gate electrode is known as mid-gap CMOS technology.

[0002] In addition, the contact surface of the gate electrode is actually provided by a silicide layer ($TiSi_2$, $CoSi_2$, $PtSi_2$, PtSi or NiSi) on top of the polycrystalline Si gate (e.g. n+-Si) in current CMOS fabrication processes. At relatively high temperatures (e.g. 600°C), the silicide film is usually degraded by two phenomena: inversion and agglomeration. Inversion is due to the grain growth of Si during the formation of

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